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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

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of

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Complete if Known				
Application Number	09/849736			
Filing Date	05/04/01			
First Named Inventor	G. Glenn Henry			
	Thomas C. McDonald			
Group Art Unit	2183			
Examiner Name	David Huisman			
Attorney Docket Number	CNTR.2021			

U.S. PATENT DOCUMENTS U.S. Patent Document Date of Publication									
Examiner Initiats	Cite No.'	U.S. Patent D Number	Kind Code ²	Name of Palentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear			
101	AA	5142634		Fite et al	08/25/1992				
077	AB	5163140		Stiles et al	11/10/1992				
1021	AC	5404467		Saba et al	04/04/1995				
ODA	AD	5687360		Po-Hua Chang	11/11/1997				
007}	ΑE	5761723		Black et al	06/02/1998				
Ont	AF	5867701		Brown et al	02/02/1999				
1001	AG	5964868		Gochman et al	10/12/1999	-			
ant	AH	5974543		Hilgendorf et al	10/26/1999				
mt	Al	5978909		Oded Lempel	11/02/1999				
tica	AJ	6088793		Liu et al	07/11/2000				
(D)	AK	6151671		D'Sa et al	11/21/2000				
M	AL	6314514		Thomas C. McDonald	11/6/2001				
fa0)	AM	6502185		Keller et al	12/31/2002				
400	AN	6601161		Rappoport et al	07/29/2003	· ·			
#100	AO	6647467		Eric M. Dowling	11/11/2003				
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	OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS						
Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²				
1007H	ВА	YEH ET AL; <u>ALTERNATIVE IMPLEMENTATION OF TWO-LEVEL ADAPTIVE BRANCH PREDICTION;</u> 19 ^{1H} Annual International Symposium on Computer Architecture, pp. 124-134, May 19-21, 1992, Gold Coast, Australia.					
DOH	ВВ	CHANG ET AL; ALTERNATIVE IMPLEMENTATIONS OF HYBRID BRANCH PREDICTORS; Proceedings of MICRO-28, 1995, IEEE.					
6004	ВС	MC FARLING, SCOTT; WRL TECHNICAL NOTE TN-36, "Combining Branch Predictors, June 1993, Western Research Laboratory, 250 University Ave., Palo Alto, CA 94301					
007H	BD	IEEE 100; THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS; Seventh Edition, IEEE, Standards Information Network, IEEE Press,					
02X	BE	BRAY ET AL; STRATEGIES FOR BRANCH TARGET BUFFERS; Technical Report No. CSL-TR-91-480, June 1991.					

	Examiner Signature	Did	1. Admin	Date Considered	1-14-05
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Substitute for form 1449A/PTO Complete if Known 09/849736 **Application Number INFORMATION DISCLOSURE** Filing Date 05/04/01 STATEMENT BY APPLICANT **First Named Inventor** G. Glenn Henry Thomas C. McDonald (use as many sheets as necessary Group Art Unit 2183 **Examiner Name David Huisman** Sheet 1 **Attomey Docket Number** CNTR.2021

Exami	Cite	U.S. Patent Doo	cument	Name of Patentee or Applicant	Date of Publication of	Pages, Columns, Lines, Where Relevan
ner Initial s	No.1	Number	Kind Code ²	of Cited Document	Cited Document MM-DD-YYYY	Passages or Relevant Figures Appear
(D)	AA	5355459		Matsuo et al	10/11/1994	
400	AB	5850543		Shiell et al	12/15/1998	
007Y	AC	6108773		Col et al	08/22/2000	
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	FOREIGN DATENT DOCUMENTS							
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	OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS						
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000A	ВА	"Microarchitecture support for reducing Branch Penalty in a Superscaler Processor", pp 208-216; Mamoru Sakamoto et al., Mittsubishi Electric Corp., 4-1 Mizuhara, Itami, Hyogo 664, Japan, 1996 IEEE.					
100H	BB	Microprocessor Report; Intel's P6 Uses Decoupled Superscalar Design, Vol. 9, No. 2, February 16, 1995.					
00H	вс	Microprocessor Report; MicroDesigns Resources, August 23, 1999.					
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